LIBRARY ieee ;

USE ieee.std\_logic\_1164.all ;

USE ieee.std\_logic\_unsigned.all ;

ENTITY lab6b IS

PORT ( add\_sub : in std\_logic;

zero\_flag : out std\_logic;

X, Y : IN STD\_LOGIC\_VECTOR(4 DOWNTO 0) ;

Result : OUT STD\_LOGIC\_VECTOR(4 DOWNTO 0) ;

Overflow : OUT STD\_LOGIC ) ;

END lab6b ;

ARCHITECTURE Behavior OF lab6b IS

SIGNAL internal\_result : STD\_LOGIC\_VECTOR(5 DOWNTO 0) ;

BEGIN

internal\_result <= ('0'&X +Y) when add\_sub='1' else ('0' & X - Y);

Result <= internal\_result(4 downto 0);

Overflow <= X(4) xor Y(4) xor internal\_result(4) xor internal\_result(5);

zero\_flag <='1' when internal\_result(4 downto 0) = "00000" else '0';

END Behavior ;